

CLAIMS

What is claimed is :

1.A method for forming a junction region of a
5 semiconductor device, said method comprising:

providing a semiconductor substrate;

forming a gate structure on said semiconductor
substrate;

10 implanting a dopant into said semiconductor
substrate to form a junction region;

forming an insulator layer on said gate structure and
said semiconductor substrate;

performing a carbon-containing plasma treatment for
said insulator layer; and

15 performing a heat treatment for said semiconductor
substrate.

2.The method of claim 1, further comprising:

forming a spacer on a side-wall of said gate structure;

20 and

implanting said dopant to form a source/drain region
next to said junction region.

3.The method of claim 2, wherein the step of forming
25 said spacer comprises:

conformally forming a nitride layer on said insulator

layer; and

removing a portion of said nitride layer and said insulator layer to form said spacer.

5 4.The method of claim 1, wherein said junction region has a thickness of about less than 400 angstroms.

10 5.The method of claim 1, wherein said carbon-containing plasma comprises using a source containing carbon dioxide gas.

15 6.The method of claim 1, wherein said carbon-containing plasma utilizes a power on the order of 0.1 to 0.5 w/cm².

7.The method of claim 1, wherein the step of forming said insulator layer comprises conformally forming a liner oxide.

20 8.The method of claim 1, wherein said dopant is at least selected from the group consisting of one group III and group V element.

25 9.The method of claim 1, wherein said carbon-containing plasma is performed to penetrate carbon atoms into said junction region, and the concentration of said

carbon atoms in said junction region is around above $1 \times 10^{19}/\text{cm}^3$.

10. The method of claim 1, wherein the temperature of
5 said heat treatment for said semiconductor substrate is about 500 to 1200°C.

11. The method of claim 1, wherein said heat treatment
is selected from the group consisting of a furnace
10 annealing treatment and a rapid thermal annealing treatment.

12. A treatment method for forming junctions of a semiconductor device, said method comprising:

- 15 providing a silicon substrate;
- forming a gate structure on said silicon substrate;
- forming a first spacer on a side-wall of said gate structure;
- implanting a dopant of boron into a portion of said
- 20 silicon substrate to form a first doped region;
- forming an oxide liner on said first spacer, said gate structure and said silicon substrate;
- performing a carbon-containing plasma treatment for said oxide liner;
- 25 forming a second spacer on said first spacer;
- implanting a dopant of p-type into said portion of said

silicon substrate to form a second doped region next to said first doped region;

performing a rapid thermal annealing treatment for said silicon substrate; and

5 forming a silicide layer on said gate structure and said silicon substrate.

13.The method of claim 12, wherein said first doped region has a thickness of about less than 400 angstroms.

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14.The method of claim 12, wherein said carbon-containing plasma comprises using a source containing carbon dioxide gas.

15 15.The method of claim 12, wherein said carbon-containing plasma utilizes a power on the order of 0.1 to 0.5 w/cm².

16.The method of claim 12, wherein said carbon-containing plasma is performed to penetrate carbon atoms into said first doped region, and the concentration of said carbon atoms in said first doped region is around above 1e19/cm³.

25 17.The method of claim 12, wherein said oxide liner is SiO₂.

18.The method of claim 12, wherein said second spacer is Si_3N_4 .

5 19.The method of claim 12, wherein the temperature of said rapid thermal annealing treatment for said silicon substrate is about 900 to 1200°C .

20.The method of claim 12, wherein said silicide is
10 self-aligned Co-silicide, such as CoSi_2 .